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UTILITY PATENT APPLICATION TRANSMITTAL

*Only for new nonprovisional applications under 37 C.F.R. § 1.53(b)

Attorney Docket No.	MIC 1010-009
First Inventor or Application Identifier	Curran
Title	Single Board Computer Quotation and Design System and Method
Express Mail Label No.	EL039916699US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 70231

1. [X] • Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)

2. [X] Specification [Total Pages 26]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 6]

4. Oath or Declaration [Total Pages 3]
a. [X] Newly executed (original or copy)
b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
[ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

* NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 CFR, § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28)

5. [ ] Microfiche Computer Program (Appendix)

6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. [ ] Computer Readable Copy
b [ ] Paper Copy (identical to computer copy)
c [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [ ] Power of Attorney
9. [ ] English Translation Document (if applicable)
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. [X] • Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. [ ] Other: _____

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No __ __ /__ __ __ __ __ __
Prior application information: Examiner _____ Group/Art Unit: __ __ __

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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"Express Mail" Number: EL039916699US Date of Deposit: 6-7-00

Applicant: Curran, et al.
Docket No.: MIC 1010-009
Serial No.:
Filed: Herewith
For: SINGLE BOARD COMPUTER QUOTATION AND DESIGN SYSTEM AND METHOD

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.27(a)) - SMALL BUSINESS CONCERN

I hereby declare that I am

[ ] the owner of the small business concern identified below:
[x] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: Micro Industries Corporation
ADDRESS OF CONCERN: 8399 Green Meadows Drive North, Westerville, Ohio 43081-9486

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract of law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled Single Board Computer Quotation and Design System and Method by inventors: Michael A. Curran, Russell J. Diehl, Gary A. Peck, and Kevin L. Rahaman,

[X] the specification filed herewith
[ ] application Serial No. _____ filed _____

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statement are required from each person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME_____

ADDRESS_____

[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements are made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING MICHAEL A. CURRAN, PRESIDENT

ADDRESS OF PERSON SIGNING 8399 Green Meadows Drive North, Westerville, Ohio 43081-9486

SIGNATURE _____ DATE JUNE 7, 2000

APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

SINGLE BOARD COMPUTER QUOTATION AND DESIGN SYSTEM AND METHOD

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SINGLE BOARD COMPUTER QUOTATION AND DESIGN SYSTEM AND METHOD

Inventors: Michael A. Curran
Russell J. Diehl
Gary A. Peck
Kevin L. Rahaman

BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates generally to automated design systems. Particularly, the present invention relates to an automated system and method for providing an instantaneous cost quotation and design feasibility assessment of a single board computer (SBC) product based on customer specifications.

Manufacturers of sophisticated electronic equipment such as printers, copiers, medical devices, etc. often have a need to include in their products microprocessor boards that meet very specific requirements. In many cases, the manufacturers arrange for the design and production of custom boards to include in their products. However, manufacturers usually resort to custom boards only when commercially available products will not meet their needs because custom boards are more expensive than mass-marketed boards. Part of the expense can be attributed to the costs involved in evaluating various custom board designs and obtaining cost estimates for each of the design alternatives. Companies that provide custom board services often work with customers in evaluating design options and providing cost estimates. Costs associated with custom board design can be reduced, in part, if the customer can evaluate design options prior to contacting the custom design companies. A system that automates the process of evaluating design options by providing cost estimates and design feasibility could reduce the cost and lead time of providing custom board services.

The present invention is a virtual product designer that allows a user to provide specifications for a custom single board computer product and receive an instantaneous cost quotation and feasibility assessment of the product. In an example embodiment of the present invention, the user connects through the Internet to a web server adapted to accept the user's specifications for a product and to provide a cost quotation and design feasibility assessment for the specified product. Using the present invention, a user can obtain functional cost information for a custom board design very quickly.

The present invention allows a user to take functional modules from a library and configure them into a unique design to support specific microprocessor application requirements. The functional modules consist of the design parameters necessary for the implementation of the specific functions typically associated with a microprocessor design such as processors, memory configurations, etc. The design parameters include the components necessary for the implementation of the function, along with electrical, mechanical, and cost specifications for these components. Functional modules can be combined with other functional modules or they can be combined with user-defined circuit requirements using specific compatibility algorithms to form unique designs. During this design process, the user is continually updated on the functional, electrical, mechanical and cost parameters as features are added to the design.

The present invention automates the process of providing a cost and feasibility analysis for a custom board. As a result, the process of manufacturing a custom board is streamlined and the cost of producing a custom board is reduced. Design as well as delivery time for a custom board is reduced. Consequently, the desirability and affordability of custom boards is increased.

BRIEF DESCRIPTION OF THE DRAWING(S)

Fig. 1 is a block diagram of an architecture according to an example embodiment of the present invention;

Fig. 2 is an example screen for a home page according to an example embodiment of the present invention;

Fig. 3 is an example screen for specifying features of a board level product according to an example embodiment of the present invention;

Fig. 4 is an example screen for specifying I/O controller features of a board level product according to an example embodiment of the present invention; and

Figs. 5A and 5B are a flowchart of the primary steps for providing a cost quotation and feasibility assessment for a board level product according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENT(S)

Referring to Fig.1, the architecture according to an example embodiment of the present invention is shown. The user's computer 100 connects via the Internet 102 to a web server 104 that contains a design center home page and other pages of the virtual product designer (VPD) web site through which the user interacts to take advantage of the present invention. The user's computer 100 may be equipped with a browser or other user interface software adapted to present cost and design information to the user. The web server 104 directs the user to the design center home page 106. The home page 106 contains buttons and other interactive controls and forms that provide the user with access to the functional modules that are used in the design process. The

detailed data associated with the functional modules is maintained in a relational database 112 running on a Windows NT server 110 that is isolated from the web server 104 by a firewall with tunneling 108. Information from the relational database 112 is extracted from the Windows NT server 110 by the web server 104 on a regular basis to ensure that the functional modules contain accurate and timely information.

Functional modules are used to provide a cost quotation and design feasibility assessment. A functional module lists the components that comprise a common microprocessor function. A list of possible functional modules and examples are as follows.

Table 1

Generic functional module	**Specific Examples**
Processor	Pentium, Pentium II, Pentium III, Celeron
Cache	128KB, 256KB
Chip Set	TX, BX, 815E
Memory (DRAM)	DIMM, embedded
Memory (Nonvolatile)	IDE Flash, ISA Flash
Graphics	2MB frame buffer, 4MB frame buffer, flat panel support
Expansion Busses	ISA, PCI, AGP, PC/104, PC/104+
Storage Peripherals	EDIE, floppy, SCSI
I/O Peripherals	Keyboard, mouse, serial port, parallel port, USB port, touch screen support, sound 10/100Base T Ethernet, SCSI

Each functional module has attributes associated with it. These attributes describe a relevant characteristic of the functional module. They may be used to more completely describe that functional module and may be used to determine which functional modules may be used together. Some attributes may represent empirically derived characteristics that would override one calculated by individual components.

Table 2

Generic functional module	Attribute	Examples
Processor	Generic processor type	Celeron FC
	System bus speed	66, 100, 133 MHz
	Core voltage	1.8V
	Package	BGA2
Cache	Cache size	128KB, 256KB
Chip Set	System bus speeds supported	66, 100, 133 MHz
	Processors supported (Intel validated)	Celeron FC
	Busses supported	PCI 32 bits (5), ISA (6), AGP 1X (1)
	Peripheral busses supported	EIDE, USB
	Memory types supported	SDRAM, RDRAM, EDO
	Memory size supported	1 GB, 4 DIMMs
	External cache supported	Yes or No
Memory (DRAM)	Memory type	SDRAM, RDRAM, EDO
	Memory size	1 GB, 4 DIMMs
	System bus speed	66, 100, 133 MHz
Memory (Nonvolatile)	Nonvolatile memory size	16 MB
	Bus	ISA, EIDE
	Bootable	Yes or No
Graphics	Bus	PCI, AGP
	Frame buffer size	2 MB, 4MB
	Flat panel support	Yes or No
Expansion Busses	Form factor required	Motherboard
	Bus (loads)	ISA (1), PCI(1), AGP (1)
I/O Peripherals	Bus (loads)	ISA (1), PCI(1), AGP (1)
All	Power (typical measured)	5 W
	Size (measured)	2.5 square inches
	Panel area (measured)	.85 square inches

Referring to Fig. 2, an example screen for a home page according to an example embodiment of the present invention is shown. The user determines the functions on the home page 120 that are critical to the application requirements and selects from function blocks (Form Factor Blocks 122, Processor Blocks 124, Chip Set Blocks 126,

Memory Blocks 128, Graphics Controller Blocks 130, Peripheral Controller Blocks 132, I/O Controller Blocks 134) in order of their priority. For example, the application may have certain performance objectives but the form factor may not be critical, therefore, the user can specify various processor types to evaluate the cost impacts of the selections without defining the form factor requirements.

Referring to Fig. 3, an example screen for specifying features of a board level product according to an example embodiment of the present invention is shown. As the user continues to define the functional requirements of the product, the VPD updates a product features window 144 and a design feasibility window 146 of the page 140. The product features window 144 lists the function blocks that have been selected for the product. The user can review a detailed specification for a function block at any time by simply double clicking on the selected block. The design feasibility window 146 provides the mechanical characteristics of the product (component density), the electrical requirements (power dissipation), and the product costs (estimated costs). Finally, a disclaimer area window 148 may be used to tell the user about any assumptions or special considerations that factor into the cost quotation or feasibility assessment provided by the system.

The following example illustrates the method that can be used to define a unique product requirement. To initiate the design for a custom form factor with a Pentium processor, the user selects a form factor block 122 from the home page shown in Fig. 2. The VPD responds by providing the user with three windows 142, 144, 146 as shown in Fig. 3. The first window is the inquiry window 142 where the user can select the form factor that supports the application requirement. The products feature window 144 lists

the functional modules that have been selected by the user. The design feasibility window 146 provides the current feasibility analysis.

As shown in Fig. 3, the user may select from any one of several form factors that are listed in the menu of the inquiry window 142. If the user is creating a custom form factor, the user may select "Custom" from the menu of the inquiry window 142. Next, the user is asked to define the length and width of the custom printed circuit board and the area that is required for panel mount connectors. The user moves from one data field to another by pressing the tab key. When all the data is complete, the user can press the enter key to enter the information into the list of functional modules and move to the next function block. Alternatively, the user can click on the desired function block in the list in the product features window 144 to obtain the inquiry window for the selected block. The user may at any time go back and change the product features by clicking on the desired block. As soon as the form factor is entered into the product features list, the information in the design feasibility window 146 is updated. The user may also review the detailed specifications for a functional module, at any time, by clicking on the selected functional module in the product features list of the product features window 144.

Referring to the product features window 144 of Fig. 3, after the form factor, the next functional module selected by the user is the processor block. The inquiry window 142 advances and the user is given a list of the standard processors that are currently supported. The user may select, for example, a Pentium. The VPD requests the user to select an operating frequency. By clicking the desired frequency and pressing the enter key, the information is added to the product feature list in the product features

window 144 and the design feasibility window 146 is updated. Based on the processor selection, a compatible chip set is the Intel TX chip set, so this selection automatically appears in the product feature list of the product features window 144. The user can change the chip set by clicking the chip set block in the product features list of the product features window 144. If the user desires to select another chip set that is not compatible with the Pentium processor, the Pentium processor may be deleted from the product features list to obtain a complete list of available chip sets.

Referring to the product features window 144 of Fig. 3, with the processor and the chip set specified, the user next selects the options from the memory block. The inquiry window 142 advances and the user is given a list of memory options or specifications. If the application requires high reliability, the user may select an on-board memory option with support for 32MB of SDRAM and no cache memory. The application may also require additional non-volatile memory so the user may select the NVRAM option and specify an M-Systems flash memory site with no memory installed. The user presses the enter key and the information is entered into the product features list of the product features window 144. The design feasibility window is updated and the inquiry window 142 advances to the graphic controller block. The available graphic controllers are displayed in the inquiry window 142 along with the options associated with each controller. The user may select, for example, the Asiliant 69000 with the LCD and Video support options. This information is entered and the VPD advances to the peripheral controller requirements.

In the inquiry window 142, the peripheral controller block provides a variety of options such as single or multiple EIDE interfaces, SCSI interface, floppy disk interface

and single or multiple USB ports. The user may select the options or specifications required for the application with the VPD insuring that the selected options are compatible. In this example, the user selects a single EIDE interface, a floppy interface, and two USB interfaces by clicking on the options and entering the data into the product feature list and the design feasibility window.

The final block is the I/O controller block. Referring to Fig. 4, an example screen for specifying I/O controller features of a board level product according to an example embodiment of the present invention is shown. The user has a large number of options to select from in the inquiry window 152 and each option contains configuration data that allows the user to select the appropriate interface requirements for the application. For example, the user may decide to configure the product with two serial I/O ports but wants one of the ports configured with an RS-232 interface and the second configured with a RS-422 interface. As the user selects additional I/O options, for example, a 10/100 Base-T Ethernet interface, the VPD ensures that the selected option does not conflict with the design guidelines for the various internal communication interfaces that are required to connect the graphic, peripheral and I/O controller blocks to the chip set and processor. Fig. 4 further illustrates the information displayed in the product features list of the product features window 154 and the design feasibility window 156 once all of the functional modules are selected. At this point, the user may print out the configuration information in the product features window 154 and the design feasibility window 156 along with the detailed description for each of the standard functional modules. The user also has the option of saving the information in a private directory for future reference or submitting the information to the NT server to obtain a detailed

analysis of the non-recurring engineering costs that would be required to implement the product and generate initial prototype units.

As indicated in Figs. 2, 3 and 4, the present invention uses customer queries (e.g., questions, menus, forms, etc.) to determine the specifications for the custom product the user would like to build. The user may be prompted to select among several options that may be available. The information provided by the user is used to build a bill of materials (BOM) for a cost quotation. The BOM pulls individual part information (e.g., cost, power, size, lead time, placement, etc.) from the relational database to create a quote. The database may be updated regularly to provide current information that is particularly important in determining a cost.

When a customer designates a particular feature or function that is to be included on the board to be quoted (e.g., by selected a particular option), a functional module is identified. The functional modules represent groups of parts that belong to a particular function (i.e., processor, chip set, or peripheral) and are used to build the BOM. The VPD enforces rules and restrictions regarding what functional modules may be used together. With this information, the VPD is able to establish a level of feasibility for the quoted design. Well-known designs may have attributes (such as power dissipation and PCB area, for example) established at the functional module level by empirical methods.

The database for the VPD comprises parts that may be referenced by number. The use of a part number allows access to existing part data such as cost and availability. Each part may have the following attributes.

Material Cost – cost of a component at multiple annual volume levels to provide a good estimation for most designs.

Assembly Cost –assembly labor cost for the component. This value may be multiplied by factors determined by assembly technique (i.e., single or double sided) or component density.

Overhead Profit – additional cost used to compute total cost.

Total cost – sum of material cost, assembly cost, and overhead profit.

Lead Time – lead time for a component. Worst case lead time of all components in a BOM is used as the assembly component lead time.

Minimum Buy – minimum buy quantity for a component.

Power – requirements for power for typical and worst case dissipation.

Size – component dimensions of length, width, and height. The length and width may include any keep out area. For a case in which a device and its socket appear on the same BOM, the socket length and width is the dimension of the socket minus the dimension of the device in the socket. The height is the maximum component height.

The length and width may be used to calculate a component area. The sum of component areas may be compared with the usable component area on a standard form factor board. The user may be given an indication of the component density of the design. The calculated density may also indicate the need for progression from a single sided board, to back side passives only, or to double sided board assemblies. The configuration is a factor in determining the assembly labor for the design.

The length and width dimensions may also be used to check if the component will fit on a standard form factor. The maximum of the component length and width may

also be compared to the maximum dimension of the board. If the component is larger than the board, it cannot be used on the board. The height may be compared to the maximum component height allowable for a form factor. Rules and restrictions may be used to disallow the use of particular components on a particular form factor.

Panel Area – total area based on length, width, and height. If a component is usually protruding through a panel, then the width and height that the component uses on the panel may be noted. This information may be used to determine if the number of selected panel components exceeds the space available on the panel for the form factor.

Placement Type – indicates whether a component may be mounted single sided or double sided. Generally, surface mount assemblies are placed single sided with particular passives on the back or double sided. This field designates those devices that can be back side placed on a passives on back design.

Lead Type – indicates whether a component is leaded or surface mounted. This information may be used for determining assembly labor costs.

For form factors, stored parameters in the database may include length, width, usable area, maximum component height, panel area, form factor type, and maximum slots (if applicable). The user may be asked to identify the form factor for the design to be quoted. A form factor may be selected from standard, common PC form factors such as AT, ATX, NLX, cPCI, PICMG, etc.

The form factor sets the board size and therefore, influences the board cost. When providing a quotation, a general formula for cost is $.08 to $.10 (depending on volume), times the number of layers, times the area of the board in square inches. The

number of layers for a microprocessor design generally ranges from four to eight. The number may be determined by the component density. The area for the board is known for each form factor. The form factor parameters also include the minimum board dimension and the maximum component height allowed. These parameters are used to determine if selected components will fit on a chosen form factor.

A panel area (height and width) may also be designated by a form factor choice. A user may then be warned if the sum of the area of the front panel components exceeds the available front panel area for the form factor. The form factor type and maximum slots attributes are useful for making decisions about the expansion slots that are allowable on the design. For instance, one configuration may allow only seven ISA connectors (maximum slots = 7) on an ATX type form factor (form factor type = motherboard).

Appendix A shows a summary listing of various cost data points and design parameters that may be tracked for the various components that may be used in a design. The cost information for the selected components is used to provide a cost quotation to a user. The design parameters and other information for the selected components are used to evaluate the feasibility of a design.

The VPD may comprise a plurality of software modules used to provide the features and functionality of the present invention. For example, the VPD comprises a cost quotation software module that examines the selected functional modules in relation to the selected form factor to determine a cost estimate. A design feasibility software module examines the selected functional modules in relation to the selected form factor to determine if the specified design will work. The attributes of the functional

modules are examined for compatibility with each other and to determine if they will fit the form factor. The attributes for the functional modules and form factors, therefore, provide the framework for the rules to determine the feasibility of proposed design. The user may change the selected form factor or the selected functional modules to obtain a new cost quotation.

The output or generated result of the VPD may include the following.

Estimated material cost at multiple volume levels – the sum of all component costs and the estimated PCB cost.

Estimated labor cost at multiple volume levels – the sum of all component assembly labor costs multiplied by any factors for assembly type or component density.

Estimated unit cost at multiple volume levels – the sum of material cost, labor cost, overhead, and profit.

Estimated lead time – the longest component lead time plus a manufacturing lead time of three weeks.

Estimated prototype cost at 5 pieces – the sum of all component costs, plus the estimated PCB cost times a fast turn multiplier, plus the PCB tooling over 5 units, plus overhead and profit.

Feature list – a list of the design's features compiled from the functional module attributes.

Detailed BOM – a list of all the components used on the design, grouped by functional module. Each component has cost, lead time, power, PCB area, panel area, and assembly cost. These attributes are subtotaled for each functional module and totaled for the entire design.

Referring to Figs. 5A and 5B, a flowchart of the primary steps for providing a cost quotation and feasibility assessment for a board level product according to an example embodiment of the present invention is shown. As shown in Figs. 5A and 5B, a user is prompted for information regarding the custom product for which a cost quotation and feasibility analysis is to be provided. In many instances, the user may select a response from a list of possible responses. In other cases, the user may be asked to enter specific values in response to a particular question. In the first step 160, the user is provided with options for defining a form factor, CPU or processor, chip set, memory, graphics controller, peripheral controller, and I/O controller. If the user selects a form factor in step 162, the user is next asked in step 170 to specify whether the form factor is custom. If the form factor is custom, the user enters a PCB size in step 172 and a panel size in step 174. If the form factor is not custom, the user selects a form factor from a predefined list of form factors in step 176. The user is prompted for additional criteria in step 178. In step 180, the user is asked to specify whether expansion slots are required. If yes, in step 182, the user is asked to select expansion slots from a list. If no, the user moves directly to the next step. In step 184, the user is prompted for a riser type. In step 186, the user may select a riser type from a list. If a riser is not required, the user moves directly to step 188 and is asked to select an I/O connector type. If an I/O connector is required, the user may select from a list of I/O connector types in step 190. If an I/O connector type is not required, the user moves directly to step 192 and is prompted for additional criteria.

In steps 208, 224, 226, and 228, a determination is made as to whether the user would like to select a CPU or processor, chip set, memory, graphics controller,

peripheral controller, or I/O controller. If the user selects a CPU or processor in steps 208 or 164, the user is prompted to select a CPU or processor from a list of processors. The user is prompted for the speed in step 198 and may select from a list of speeds in step 200. In step 202, the user is prompted for a cache type and in step 204 may select from a list of cache types. In step 206, the user may be prompted for additional criteria. If the user selects a chip set in steps 224 or 166, the user is prompted to select a chip set from a list of chip sets in step 210 and is prompted for additional criteria in step 212. If the user selects memory in steps 226 or 168, the user is prompted in step 214 to select a type of memory from a list of memory types. The user may be prompted for additional criteria relevant to the memory selection. For example, the user may be prompted for a memory size as in step 216 which may be selected from a list as in step 218. In step 220, the user proceeds with specifying criteria relevant to the product.

If the user selects a graphics controller in step 228, the user is prompted in step 236 to select a graphics controller from a list of graphics controllers. In step 238, the user proceeds with specifying additional criteria relevant to the product. If the user selects a peripheral controller in steps 230 or 240, the user is prompted in step 242 to select a peripheral controller from a list of peripheral controllers. The user proceeds with specifying additional criteria relevant to the product in step 244. If the user selects an I/O controller in steps 246 or 232, in step 248, the user is prompted to select an I/O controller from a list of I/O controllers. The user is prompted in step 250 to specify whether serial ports are required. If yes, the user is prompted in steps 264 through 270 to indicate the number of RS-232C and RS-422C ports to be accommodated. If no, the user is prompted in step 256 to specify whether USB ports are required. If yes, the user

specifies the number of ports in step 262. If no, the user moves directly to the step 258 and specifies whether there are additional I/O requirements to accommodate. In step 260, the user indicates whether the design is complete. If not, the user can return to earlier steps to complete the process of providing the specifications for the product. If the design is complete, in step 272, the results for the specified product are generated. The results include a cost quotation and design feasibility assessment. The user may return to the start of the process as many times as desired to obtain results for additional products. By requesting more than one quotation and assessment, the user may evaluate the tradeoffs associated with several different design choices and product configurations.

The present invention automates the process of providing cost quotation and design feasibility information for a custom board. A customer using the present invention can design a custom board and verify that the design works. More importantly, a customer can see what various features add to the cost of a custom board. Labor costs associated with providing such information to a potential customer are reduced as a result of the automation of the process. The reduced costs may be passed on to customers so that the use of custom boards is more desirable and affordable.

Although the present invention has been described in accordance with an example embodiment, it is understood that many modifications to the present invention may be made without departing from the scope of the present invention.

What is claimed is:

1. A system for designing a custom board, comprising:

a plurality of form factors;

a plurality of functional modules;

a cost quotation module for determining a cost quotation for a selected form factor in relation to selected ones of said plurality of functional modules;

a design feasibility module for determining a design feasibility for said selected form factor in relation to selected ones of said plurality of functional modules; and

a computer adapted to display said cost quotation and said design feasibility for said selected form factor in relation to selected ones of said plurality of functional modules.

2. The system of claim 1 wherein said plurality of functional modules is selected from the group consisting of processors, chip sets, memory configurations, graphics controllers, peripheral controllers, and I/O controllers.

3. The system of claim 1 further comprising a plurality of attributes for each of said plurality of functional modules.

4. The system of claim 3 wherein said plurality of attributes comprise cost parameters, a lead time parameter, a minimum buy quantity parameter, power parameters, size parameters, area parameters, placement parameters, mechanical parameters, and electrical parameters.

5. The system of claim 1 wherein said form factor is selected from the group

consisting of AT, LPX, ATX, NLX, cPCI, PICMG, and custom SBC.

6. The system of claim 1 further comprising a plurality of attributes for each of said plurality of form factors.

7. The system of claim 6 wherein said plurality of attributes for each of said plurality of form factors comprises size parameters, area parameters, a form factor type parameter, and a maximum number of slots parameter.

8. The system of claim 1 wherein said computer is adapted to display an inquiry window, a product features window, and a design feasibility window.

9. The system of claim 8 wherein said inquiry window comprises interactive controls for selecting one of said plurality of form factors.

10. The system of claim 8 wherein said products features window displays features for selected ones of said plurality of functional modules.

11. The system of claim 8 wherein said design feasibility window displays a current feasibility analysis for said selected form factor and selected ones of said plurality of functional modules.

12. The system of claim 1 wherein said cost quotation module and said design feasibility module are operational at a web server accessible via the Internet.

13. The system of claim 12 wherein said computer is adapted to connect to said web server via the Internet.

14. A method for designing a custom board comprising the steps of:

defining a plurality of form factors;

defining a plurality of functional modules;

prompting a user to select one of said plurality of form factors;

prompting a user to select at least one of said plurality of functional modules;

providing a design feasibility assessment for said selected form factor and said selected functional module; and

providing a cost quotation for said selected form factor and said selected functional module.

15. The method of claim 14 wherein the step of said prompting a user to select one of said plurality of form factors comprises the step of prompting said user to select a form factor from the group consisting of AT, LPX, ATX, NLX, cPCI, PICMG, and custom SBC.

16. The method of claim 14 wherein the step of defining a plurality of form factors comprises the step of associating a plurality of attributes with each of said plurality of form factors.

17. The method of claim 16 wherein the step of associating a plurality of attributes with each of said plurality of form factors comprises the step of associating size parameters, area parameters, a form factor type parameter, and a maximum number of slots parameter with each of said plurality of form factors.

18. The method of claim 14 wherein the step of defining a plurality of functional modules comprises the step of associating a plurality of attributes with each of said plurality of functional modules.

19. The method of claim 18 wherein the step of associating a plurality of attributes with each of said plurality of functional modules comprises the step of associating cost parameters, a lead time parameter, a minimum buy quantity parameter,

power parameters, size parameters, area parameters, placement parameters, mechanical parameters, and electrical parameters with each of said plurality of functional modules.

20. The method of claim 14 further comprising the step of prompting said user to select a second functional module.

21. The method of claim 20 further comprising the step of updating said cost quotation and design feasibility assessment based on said second functional module.

22. A method for evaluating custom board designs comprising the steps of:

prompting a user to select a plurality of functional modules;

prompting said user to specify options for said selected functional modules;

displaying in a products features window feature information for said selected functional modules and specified options;

displaying in a design feasibility window a design feasibility assessment for said selected functional modules and specified options;

determining if said user has changed said functional modules and specified options; and

updating said feature information in said products feature window and said design feasibility assessment in said design feasibility window in accordance with changes to said functional modules and specified options.

23. The method of claim 22 further comprising the step of associating a plurality of attributes with each of said plurality of functional modules.

24. The method of claim 23 wherein the step of associating a plurality of attributes

with each of said plurality of functional modules comprises the step of associating cost parameters, a lead time parameter, a minimum buy quantity parameter, power parameters, size parameters, area parameters, placement parameters, mechanical parameters, and electrical parameters with each of said plurality of functional modules.

25. The method of claim 22 further comprising the step of prompting said user to select one of a plurality of form factors.

26. The method of claim 25 wherein the step of said prompting a user to select one of a plurality of form factors comprises the step of prompting said user to select a form factor from the group consisting of AT, LPX, ATX, NLX, cPCI, PICMG, and custom SBC.

27. The method of claim 25 further comprising the step of associating a plurality of attributes with each of said plurality of form factors.

28. The method of claim 27 wherein the step of associating a plurality of attributes with each of said plurality of form factors comprises the step of associating size parameters, area parameters, a form factor type parameter, and a maximum number of slots parameter with each of said plurality of form factors.

29. The method of claim 25 further comprising the step of updating said feature information in said products feature window and said design feasibility assessment in said design feasibility window in accordance with said selected form factor.

30. The method of claim 27 further comprising the step of displaying in said design feasibility window a cost quotation for said selected functional modules and

specified options.

31. The method of claim 29 wherein the step of displaying in said design feasibility window a cost quotation comprises the steps of:

displaying a material cost for said selected functional modules and specified options;

displaying a labor cost for said selected functional modules and specified options; and

displaying an overhead and profit cost for said selected functional modules and specified options.

32. The method of claim 22 further comprising the step of displaying a production lead time in said design feasibility window.

ABSTRACT OF THE DISCLOSURE

The present invention is a virtual product designer that allows a user to provide specifications for a custom board level product and receive an instantaneous cost quotation and feasibility assessment of the product. The user may connect through the Internet to a virtual product designer to obtain a cost quotation and design feasibility assessment for a specified product. Functional modules that serve as building blocks for a custom design are defined and stored in a library. Attributes and design parameters associated with the functional modules are used to calculate a cost quotation and evaluate design feasibility. As the user changes design requirements while interacting with the virtual product designer, the user is continually updated on the relevant functional, electrical, mechanical and cost parameters.

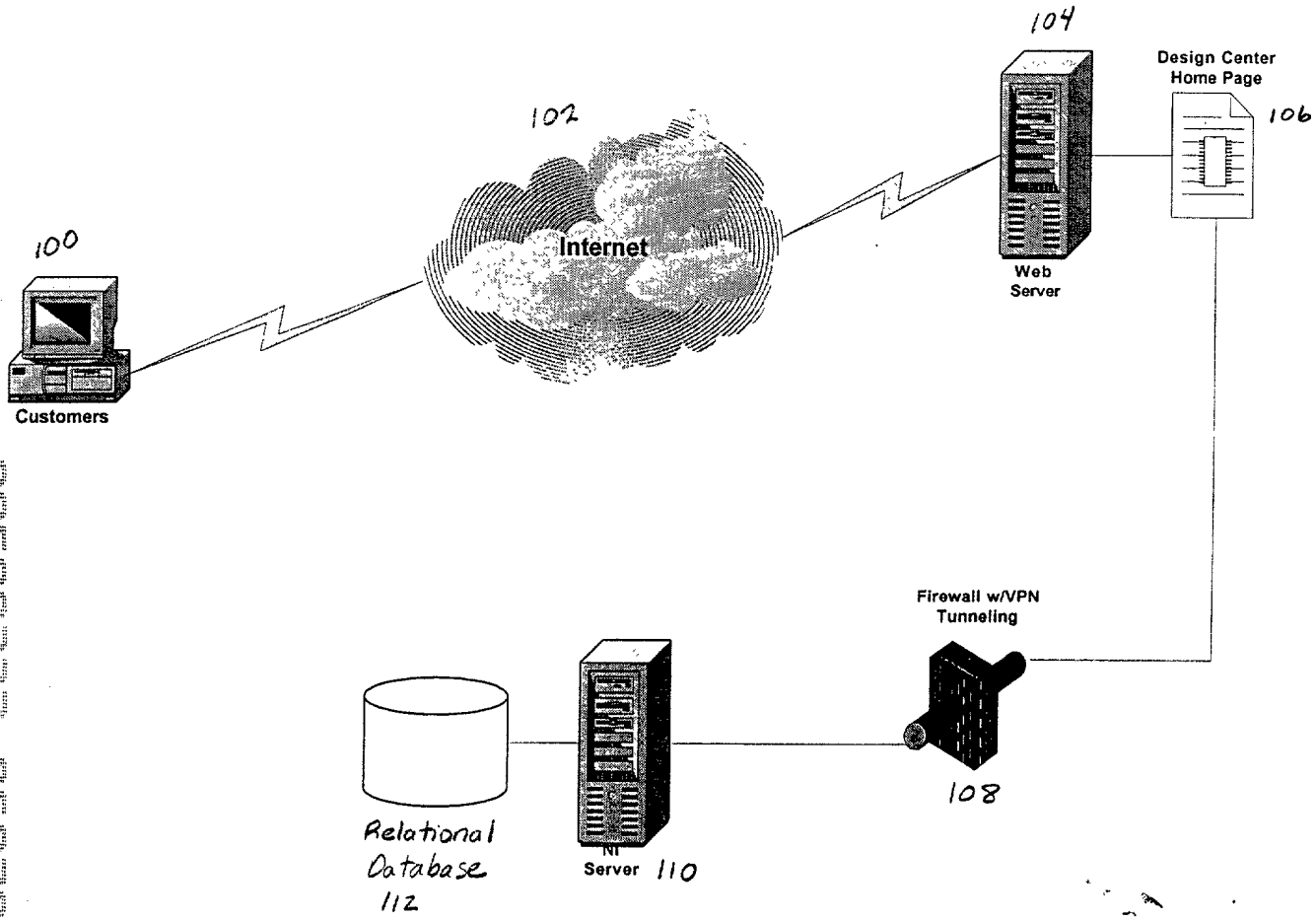

104
Design Center
Home Page
106
102
100
Internet
Web
Server
Customers
Firewall w/VPN
Tunneling
108
Relational
Database
112
NT
Server 110

Figure 1

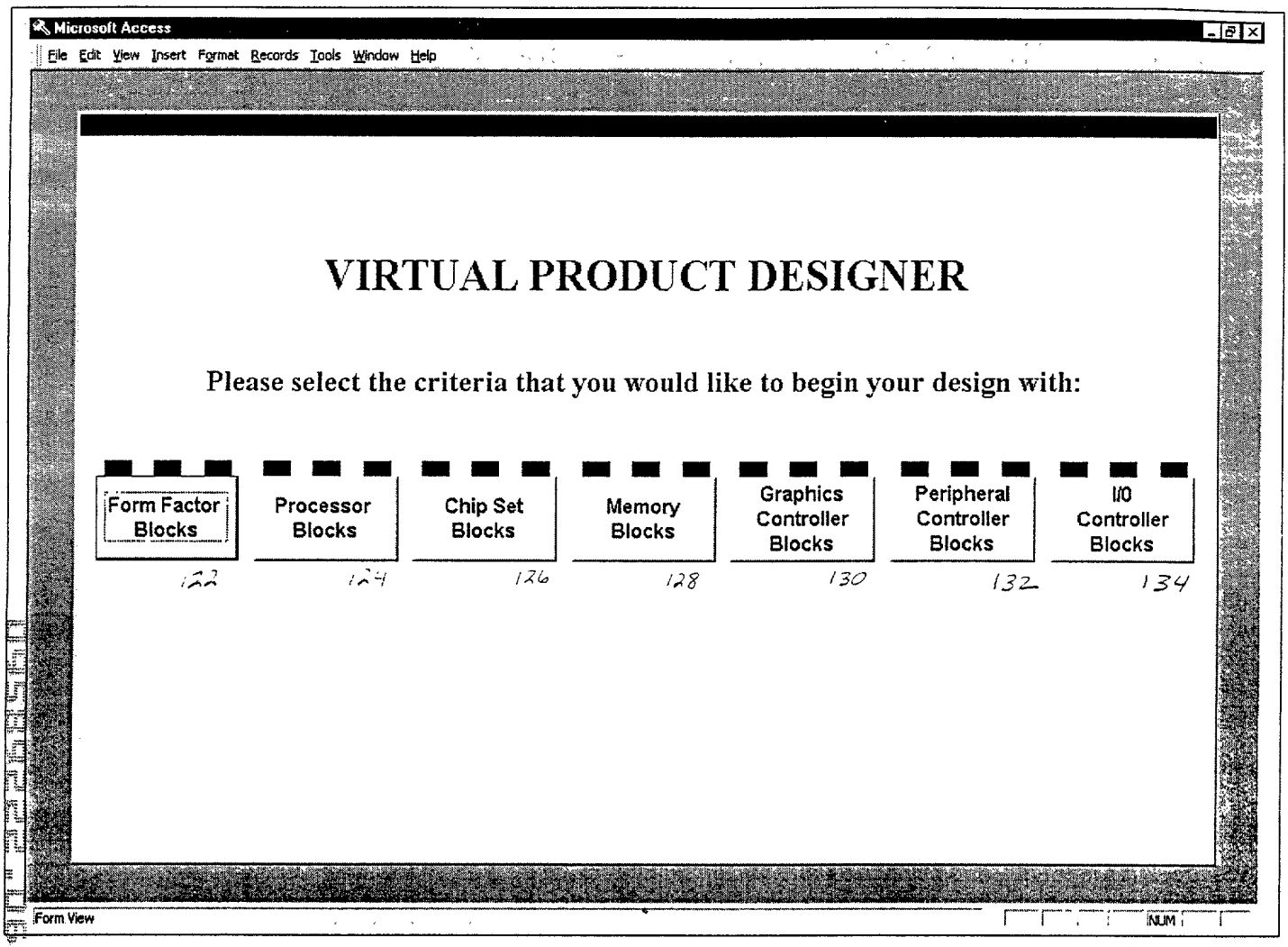

120
Microsoft Access
File Edit View Insert Format Records Tools Window Help
VIRTUAL PRODUCT DESIGNER
Please select the criteria that you would like to begin your design with:
Form Factor Blocks
Processor Blocks
Chip Set Blocks
Memory Blocks
Graphics Controller Blocks
Peripheral Controller Blocks
I/O Controller Blocks
122
124
126
128
130
132
134
Form View
NUM

Figure 2

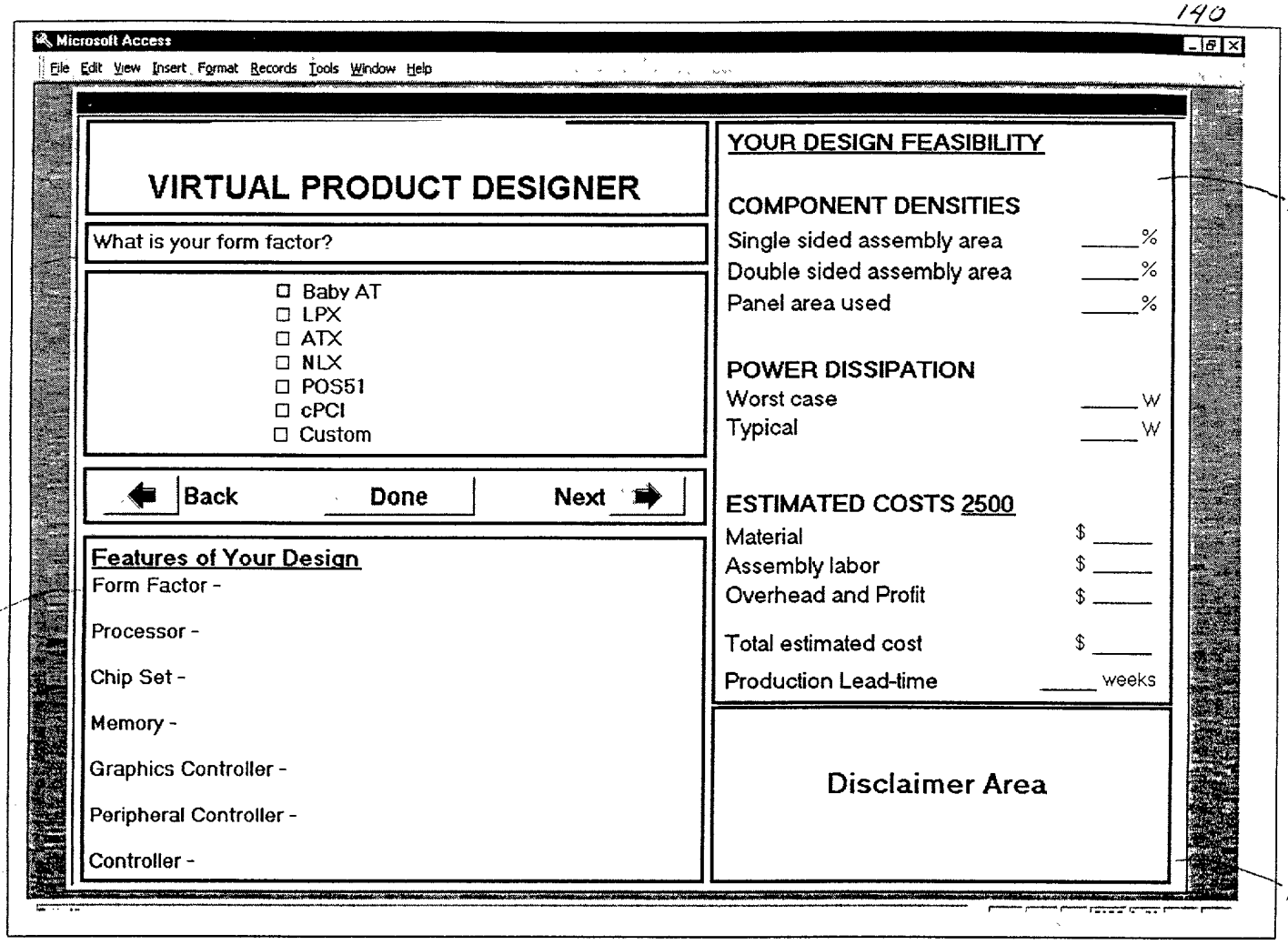

140
Microsoft Access
File Edit View Insert Format Records Tools Window Help
VIRTUAL PRODUCT DESIGNER
What is your form factor?
Baby AT
LPX
ATX
NLX
POS51
cPCI
Custom
Back
Done
Next
Features of Your Design
Form Factor -
Processor -
Chip Set -
Memory -
Graphics Controller -
Peripheral Controller -
Controller -
YOUR DESIGN FEASIBILITY
COMPONENT DENSITIES
Single sided assembly area ____%
Double sided assembly area ____%
Panel area used ____%
POWER DISSIPATION
Worst case ____W
Typical ____W
ESTIMATED COSTS 2500
Material $ ____
Assembly labor $ ____
Overhead and Profit $ ____
Total estimated cost $ ____
Production Lead-time ____ weeks
Disclaimer Area
142
144
146
148

Figure 3

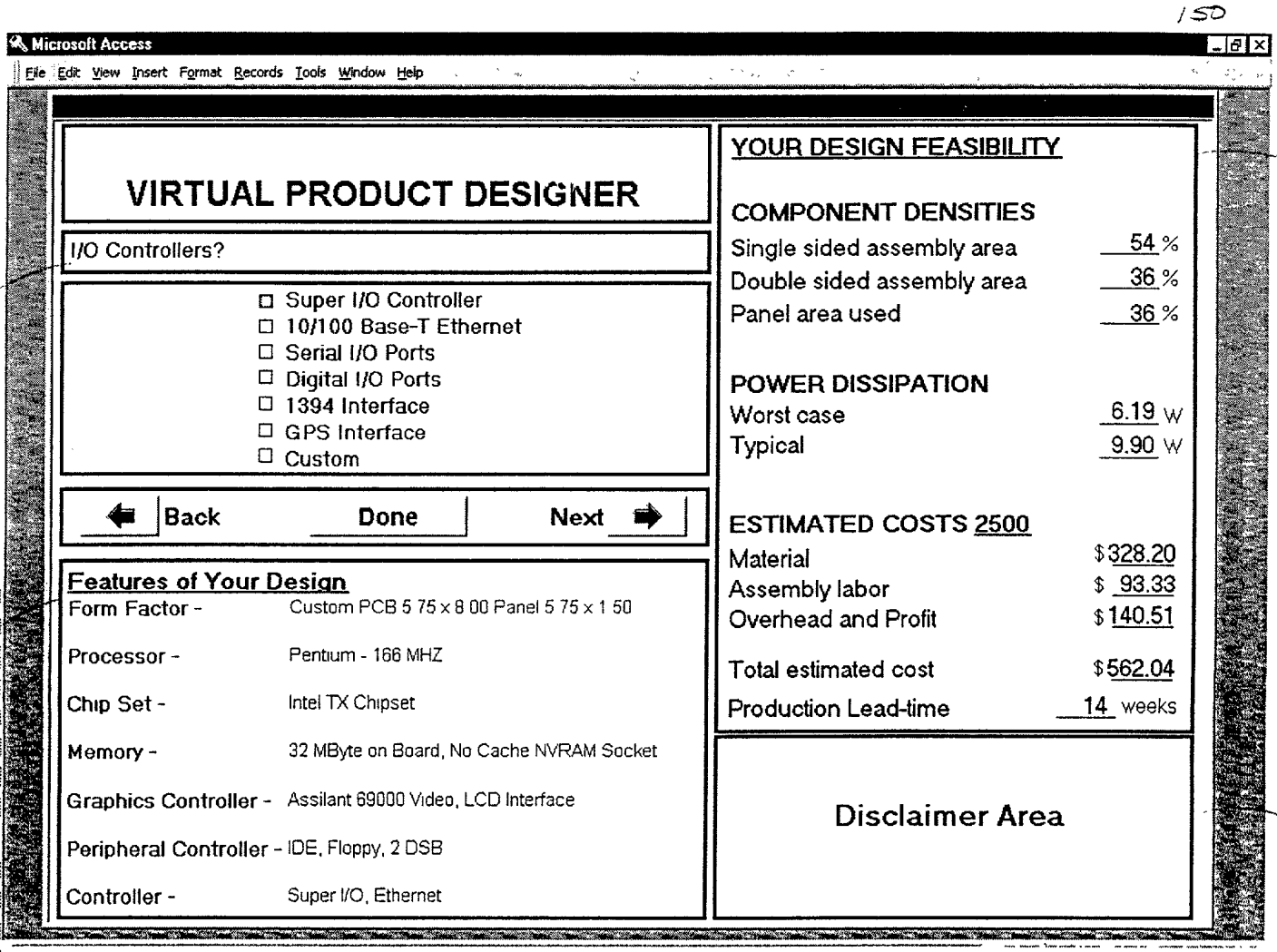

150
Microsoft Access
File Edit View Insert Format Records Tools Window Help
VIRTUAL PRODUCT DESIGNER
I/O Controllers?
Super I/O Controller
10/100 Base-T Ethernet
Serial I/O Ports
Digital I/O Ports
1394 Interface
GPS Interface
Custom
Back
Done
Next
Features of Your Design
Form Factor - Custom PCB 5 75 x 8 00 Panel 5 75 x 1 50
Processor - Pentium - 166 MHZ
Chip Set - Intel TX Chipset
Memory - 32 MByte on Board, No Cache NVRAM Socket
Graphics Controller - Assilant 69000 Video, LCD Interface
Peripheral Controller - IDE, Floppy, 2 DSB
Controller - Super I/O, Ethernet
YOUR DESIGN FEASIBILITY
COMPONENT DENSITIES
Single sided assembly area 54 %
Double sided assembly area 36 %
Panel area used 36 %
POWER DISSIPATION
Worst case 6.19 W
Typical 9.90 W
ESTIMATED COSTS 2500
Material $328.20
Assembly labor $ 93.33
Overhead and Profit $140.51
Total estimated cost $562.04
Production Lead-time 14 weeks
Disclaimer Area
152
154
156
158

Figure 4

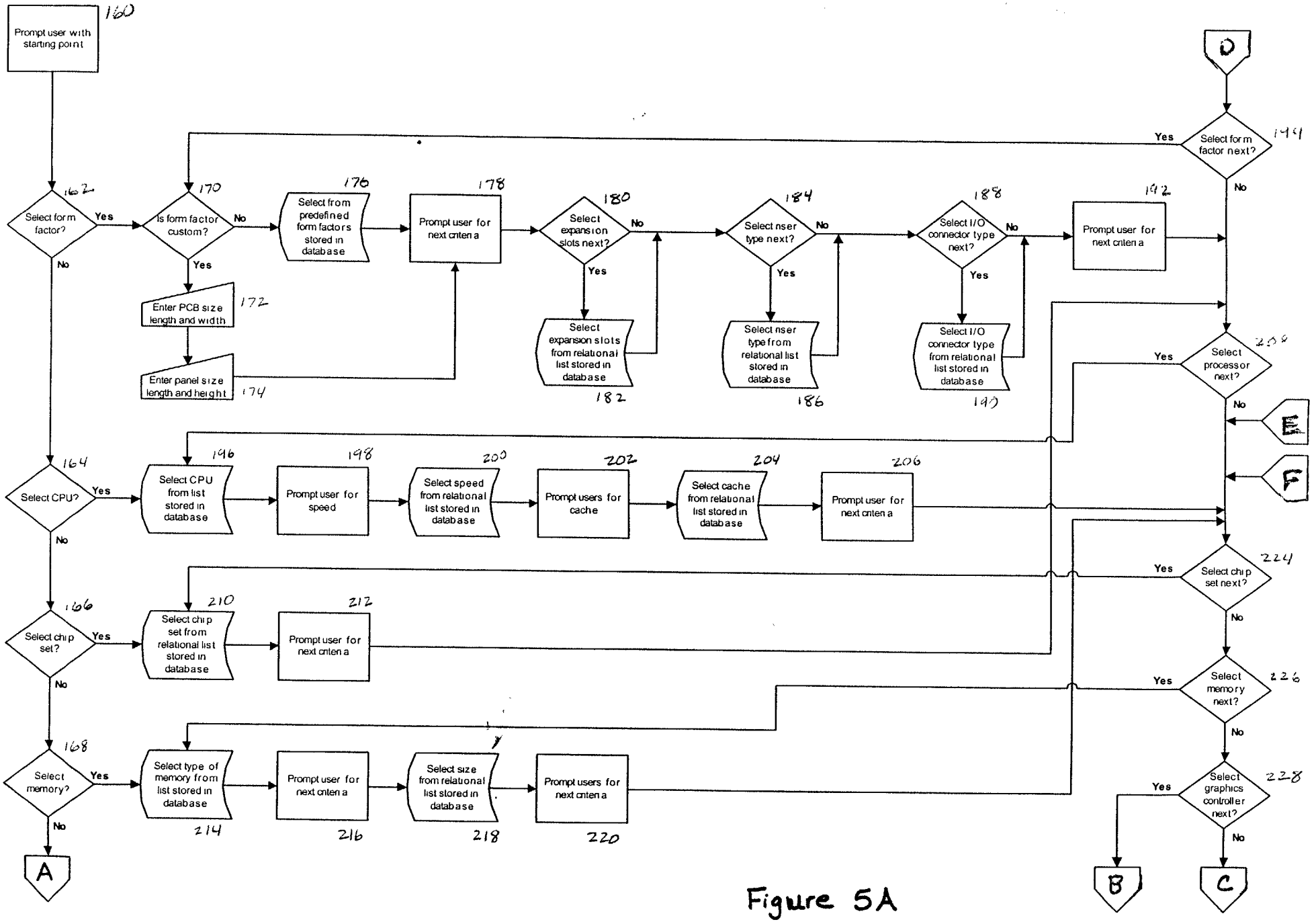

160
Prompt user with starting point
162
Select form factor?
Yes
No
170
Is form factor custom?
No
Yes
176
Select from predefined form factors stored in database
178
Prompt user for next criteria
172
Enter PCB size length and width
174
Enter panel size length and height
180
Select expansion slots next?
No
Yes
Select expansion slots from relational list stored in database
182
184
Select user type next?
No
Yes
Select user type from relational list stored in database
186
188
Select I/O connector type next?
No
Yes
Select I/O connector type from relational list stored in database
190
192
Prompt user for next criteria
D
194
Select form factor next?
Yes
No
208
Select processor next?
Yes
No
E
F
164
Select CPU?
Yes
No
196
Select CPU from list stored in database
198
Prompt user for speed
200
Select speed from relational list stored in database
202
Prompt users for cache
204
Select cache from relational list stored in database
206
Prompt user for next criteria
166
Select chip set?
Yes
No
210
Select chip set from relational list stored in database
212
Prompt user for next criteria
224
Select chip set next?
Yes
No
226
Select memory next?
Yes
No
168
Select memory?
Yes
No
Select type of memory from list stored in database
214
Prompt user for next criteria
216
Select size from relational list stored in database
218
Prompt users for next criteria
220
228
Select graphics controller next?
Yes
No
A
B
C

Figure 5A

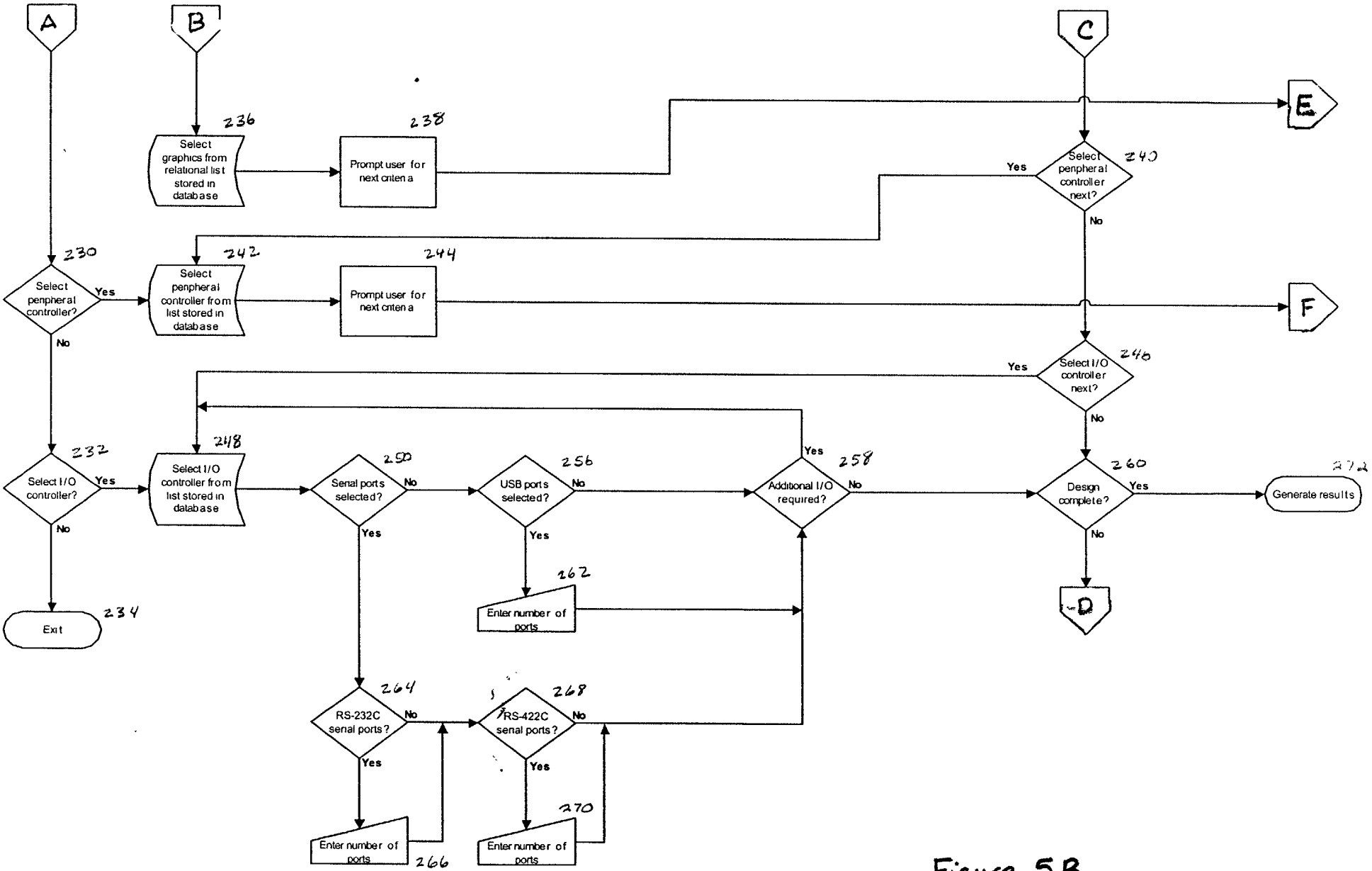

A
B
C
E
F
D
230
Select peripheral controller?
Yes
No
232
Select I/O controller?
Yes
No
234
Exit
236
Select graphics from relational list stored in database
238
Prompt user for next criteria
240
Select peripheral controller next?
Yes
No
242
Select peripheral controller from list stored in database
244
Prompt user for next criteria
246
Select I/O controller next?
Yes
No
248
Select I/O controller from list stored in database
250
Serial ports selected?
No
Yes
256
USB ports selected?
No
Yes
258
Additional I/O required?
Yes
No
260
Design complete?
Yes
No
272
Generate results
262
Enter number of ports
264
RS-232C serial ports?
No
Yes
266
Enter number of ports
268
RS-422C serial ports?
No
Yes
270
Enter number of ports

Figure 5B

Table 1

Summary of Virtual Product Designer Information

Inquiry Information		Product Feature List	Single-Sided Assembly Area	Double-Sided Assembly Area	Panel Area	Typical	Maximum	Material Cost	Assembly Cost	Overhead Profit	Total Cost	Lead Time
Form factor?			0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
	Baby AT		0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
	LPX		0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
	ATX		0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
	NLX		0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
	cPCI		0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
	Custom SBC	Custom SBC	0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
Expansion slots?			0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
	Riser	Custom SBC with a riser	0%	0%	0%	0 00	0 00	$0.00	$0 00	$0 00	$0 00	2
	PCI/ISA slots		0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
	None		0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
Riser type?			0%	0%	0%	0 00	0 00	$0 00	$0 00	$0.00	$0 00	2
	NLX		0%	0%	0%	0 00	0.00	$0 00	$0 00	$0 00	$0 00	2
	LPX		0%	0%	0%	0 00	0 00	$0 00	$0 00	$0 00	$0 00	2
	POS51	Custom SBC with a POS51 ri	3%	2%	0%	0 00	0 00	$1 00	$0 09	$0 36	$1 45	4
I/O connector type?			3%	2%	0%	0 00	0 00	$1 00	$0 09	$0 36	$1 45	4
	headers		3%	2%	0%	0 00	0 00	$1 00	$0 09	$0 36	$1 45	4
	right angle	SBC has right angle connect	4%	3%	0%	0 00	0 00	$1 25	$0 18	$0 48	$1 91	4
PCB Size L=_____inches, W=______inches			4%	3%	0%	0 00	0 00	$1 25	$0 18	$0 48	$1 91	4
	L = 5.75, W = 8 00		4%	3%	0%	0 00	0 00	$36 25	$0 18	$12 14	$48 57	10
Panel size L=_____inches, H =______inches			4%	3%	0%	0 00	0 00	$36 25	$0 18	$12 14	$48 57	10
	L = 5 75, H = 1 50		4%	3%	0%	0 00	0 00	$46 25	$0 63	$15 63	$62 51	10
Processor?			4%	3%	0%	0 00	0 00	$46 25	$0 63	$15 63	$62 51	10
	Pentium	Processor - Pentium	5%	3%	0%	0 00	0.00	$71 25	$2 43	$24 56	$98 24	12
	Celeron		5%	3%	0%	0 00	0 00	$71 25	$2 43	$24 56	$98 24	12
	Pentium II		5%	3%	0%	0 00	0 00	$71 25	$2 43	$24 56	$98 24	12
	Pentium III		5%	3%	0%	0 00	0 00	$71 25	$2 43	$24 56	$98 24	12
Speed?			5%	3%	0%	0 00	0 00	$71 25	$2 43	$24 56	$98 24	12
	166 MHz	Processor - 166 MHz Pentiu	11%	9%	0%	0 00	6 00	$129 25	$12 78	$47 34	$189 37	12
	266MHz		11%	9%	0%	0 00	6 00	$129 25	$12 78	$47 34	$189 37	12
Cache?			11%	9%	0%	0 00	6 00	$129 25	$12 78	$47 34	$189 37	12
	None	No cache	11%	9%	0%	0 00	6 00	$129 25	$12 78	$47 34	$189 37	12
	128KB		11%	9%	0%	0.00	6 00	$129 25	$12 78	$47 34	$189 37	12
	256KB		11%	9%	0%	0 00	6 00	$129 25	$12 78	$47 34	$189 37	12
Chip set?			11%	9%	0%	0 00	6 00	$129 25	$12 78	$47 34	$189 37	12
	TX	Intel TX chip set	30%	21%	0%	0 00	8 00	$186 25	$48 78	$78 34	$313 37	14
	BX		30%	21%	0%	0 00	8 00	$186 25	$48 78	$78 34	$313 37	14
Memory			30%	21%	0%	0 00	8 00	$186 25	$48 78	$78 34	$313 37	14
DRAM?			30%	21%	0%	0 00	8.00	$186 25	$48 78	$78 34	$313 37	14
	On board	DRAM - SDRAM on board	30%	21%	0%	0 00	8 00	$186 25	$48 78	$78 34	$313 37	14
	Module		30%	21%	0%	0 00	8 00	$186 25	$48 78	$78 34	$313 37	14
Size?			30%	21%	0%	0 00	8.00	$186 25	$48 78	$78 34	$313 37	14
	32MB	DRAM - 32MB SDRAM on bo	34%	23%	0%	0 00	9 00	$236 25	$57 78	$98 01	$392 04	14
	64MB		34%	23%	0%	0 00	9 00	$236 25	$57 78	$98 01	$392 04	14
	96MB		34%	23%	0%	0.00	9 00	$236 25	$57.78	$98 01	$392 04	14
	128MB		34%	23%	0%	0 00	9 00	$236 25	$57 78	$98 01	$392 04	14
NVRAM?			34%	23%	0%	0 00	9 00	$236 25	$57 78	$98 01	$392 04	14
	M Systems FLASH site	M Systems FLASH site	36%	24%	0%	0 00	9 00	$236 50	$57 96	$98 15	$392 61	14
	FLASH card site		36%	24%	0%	0 00	9 00	$236 50	$57 96	$98 15	$392 61	14
Graphics Controllers?			36%	24%	0%	0 00	9 00	$236 50	$57 96	$98 15	$392 61	14
	2MB frame buffer	Graphics accelerator with 2M	43%	29%	0%	0 00	9 50	$281 50	$65 16	$115 55	$462 21	14
	4MB frame buffer		43%	29%	0%	0 00	9 50	$281 50	$65 16	$115 55	$462 21	14
Flat panel support?			43%	29%	0%	0 00	9 50	$281 50	$65 16	$115 55	$462 21	14
	Yes	Supports flat panel displays	45%	30%	5%	0 05	9 50	$286 50	$66 96	$117 82	$471 28	14
	No		45%	30%	5%	0 10	9 50	$286 50	$66 96	$117 82	$471 28	14
Peripheral Controllers?			45%	30%	5%	0 15	9 50	$286 50	$66 96	$117 82	$471 28	14
EIDE?			45%	30%	5%	0 20	9 50	$286 50	$66 96	$117 82	$471 28	14
	Yes, one connector	EIDE connector	46%	31%	5%	0 25	9 50	$288 50	$72 81	$120 44	$481 75	14
	Yes, two connectors		46%	31%	5%	0 30	9 50	$288 50	$72 81	$120 44	$481 75	14

No		46%	31%	5%	0.35	9 50	$288 50	$72 81	$120 44	$481 75	14
USB?		46%	31%	5%	0.40	9 50	$288 50	$72 81	$120 44	$481.75	14
Yes, one port		46%	31%	5%	0 45	9 50	$288 50	$72 81	$120 44	$481 75	14
Yes, two ports	Two USB ports	47%	31%	8%	0 53	9 50	$290 50	$76 41	$122 30	$489 21	14
No		47%	31%	8%	0 61	9 50	$290 50	$76 41	$122 30	$489 21	14
SCSI?		47%	31%	8%	0 68	9 50	$290 50	$76 41	$122 30	$489 21	14
SCSI-2		47%	31%	8%	0 76	9 50	$290 50	$76 41	$122 30	$489 21	14
Ultra SCSI-2		47%	31%	8%	0 84	9.50	$290 50	$76 41	$122 30	$489 21	14
Floppy?		47%	31%	8%	0 92	9 50	$290.50	$76 41	$122.30	$489 21	14
Yes		47%	31%	8%	0 99	9.50	$290 50	$76 41	$122 30	$489 21	14
No		47%	31%	8%	1 07	9 50	$290 50	$76 41	$122 30	$489 21	14
I/O Controllers?		47%	31%	8%	1 15	9 50	$290 50	$76 41	$122 30	$489 21	14
Super I/O controller		47%	31%	8%	1 23	9 50	$290 50	$76 41	$122 30	$489 21	14
Senal port		47%	31%	8%	1 31	9 50	$290 50	$76 41	$122 30	$489 21	14
Number of RS-232C senal ports = _______		47%	31%	8%	1 38	9 50	$290 50	$76 41	$122 30	$489 21	14
Number of RS-232C senal	RS-232C senal port	48%	32%	13%	1 51	9 70	$295.50	$79 56	$125.02	$500 08	14
Number of RS-422C senal ports = _______		48%	32%	13%	1 64	9 70	$295 50	$79 56	$125 02	$500 08	14
Number of RS-422C senal	RS-422 senal port	49%	33%	18%	1 82	9 90	$301 50	$82 71	$128 07	$512 28	14
Parallel port	Parallel port	50%	34%	29%	2 11	9 90	$303 50	$87 21	$130 24	$520 95	14
Floppy controller	Floppy controller	51%	35%	29%	2 39	9 90	$304 00	$90 45	$131 48	$525 93	14
Keyboard	PS/2 keyboard port	52%	35%	32%	2 71	9 90	$304 70	$91 08	$131 93	$527 71	14
Mouse	PS/2 mouse port	52%	35%	32%	3 03	9 90	$304 70	$91 08	$131 93	$527 71	14
10/100 BaseT ethernet		52%	35%	32%	3.34	9 90	$304 70	$91 08	$131 93	$527 71	14
Quantity _____	10/100 BaseT ethernet	52%	35%	32%	3 66	9 90	$304 70	$91 08	$131 93	$527 71	14
Quantity of Ethernet ports = 1		54%	36%	36%	4 02	9 90	$328 20	$93 33	$140.51	$562 04	14
Senal I/O ports		54%	36%	36%	4.38	9 90	$328.20	$93 33	$140 51	$562 04	14
Number of RS-232C senal ports = _______		54%	36%	36%	4 74	9 90	$328 20	$93 33	$140 51	$562 04	14
Number of RS-422C senal ports = _______		54%	36%	36%	5 11	9 90	$328 20	$93 33	$140 51	$562 04	14
Digital I/O interface		54%	36%	36%	6 19	9 90	$328 20	$93 33	$140 51	$562 04	14
Number of Digital I/O ports = _______		54%	36%	36%	6 55	9 90	$328 20	$93 33	$140 51	$562 04	14
Digital I/O termination		54%	36%	36%	6 91	9 90	$328 20	$93 33	$140 51	$562 04	14
1394 Interface		54%	36%	36%	5 47	9 90	$328 20	$93 33	$140 51	$562 04	14
GPS Interface		54%	36%	36%	5 83	9 90	$328 20	$93 33	$140 51	$562 04	14
Complete		54%	36%	36%	6 19	9.90	$328 20	$93 33	$140 51	$562 04	14

Express Mail No.: EL039916699US **Date of Deposit:** June 7, 2000

DECLARATION
AND
POWER OF ATTORNEY

As below named inventors, we hereby declare that:

Our residences, post office addresses and citizenship are as stated below next to our names.

We believe we are the original, first, and joint inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled SINGLE BOARD COMPUTER QUOTATION AND DESIGN SYSTEM AND METHOD the specification of which:
(check one) [X] is attached hereto.

[ ] was filed _____ as
Application Serial No. _____
and was amended on _____ (if applicable).

We hereby state that we have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

We acknowledge the duty to disclose information which is material to the patentability of the invention claimed in this application, in accordance with Title 37, Code of Federal Regulations, §1.56(a) and (b).

We hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No

We hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of

Title 35, United States Code, §112, we acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulation, §1.56(a) and (b) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending abandoned)

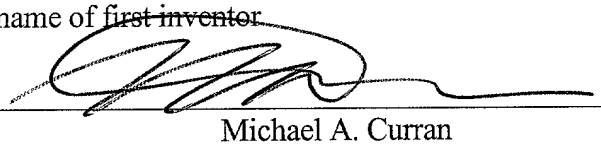
We hereby claim the benefit under 35 U.S.C. 119(e) of any United States Provisional Application listed below:

None	
(Application Serial No.)	(Filing Date)

We hereby appoint Jeffrey S. Standley, Reg. No. 34,021, Carol G. Stovsky, Reg. No. 42,171, James L. Kwak, Reg. No. 41,133, Jeffrey C. Norris, Reg. No. 42,039, c/o Standley & Gilcrest LLP, 495 Metro Place South, Suite 210, Dublin, Ohio 43017-5315, Telephone No. (614) 792-5555 our attorneys, with full power in each of them, of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith. All correspondence should be sent to the attention of **Jeffrey S. Standley, Esq.** at the address above.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of ~~first inventor~~



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